

CLAIMS

1        1. A method comprising:

2              analyzing characteristics of signals passing along a first plurality of conductive paths arranged

3        in a first orientation; and

4              determining a second orientation for a second plurality of conductive paths based on said

5        analyzed characteristics.

1        2. The method of claim 1, wherein said characteristics comprise timing relationships of

2        signals across said first plurality of conductive paths.

1        3. The method of claim 2, wherein said timing relationships relate to one of push-out and

2        pull-in of signal timings.

1        4. The method of claim 1, wherein said first plurality of conductive paths are on a first

2        plane and arranged in said first orientation and said second plurality of conductive paths are on a

3        second plane and arranged in said second orientation.

1        5. The method of claim 1, wherein said first plurality of conductive paths comprise a first

2        plurality of traces on a first layer of a printed circuit board and said second plurality of conductive paths

3        comprise a second plurality of traces on a second layer of said printed circuit board.

1        6. The method of claim 5, wherein said first plurality of traces are arranged on said first

2        layer in a first ordered arrangement and said second plurality of traces are arranged on said second

3 layer in a second ordered arrangement, and determining said second orientation comprises  
4 determining said second ordered arrangement based on the analyzed characteristics.

1           7. The method of claim 1, wherein said first plurality of conductive paths comprise a first  
2 plurality of vias coupling a first layer of a printed circuit board to a second layer of said printed circuit  
3 board, and said second plurality of conductive paths comprise a second plurality of vias coupling said  
4 first layer of said printed circuit board to said second layer of said printed circuit board.

5           8. A method of designing a printed circuit board comprising:  
6           analyzing at least one characteristic of a first plurality of relatively parallel conductive paths on  
7           said printed circuit board, said first plurality of relatively parallel conductive paths being arranged in a  
8           pattern in a first area of said printed circuit board; and  
9           rearranging said pattern of conductive paths such that a second plurality of relatively parallel  
10          conductive paths in a second area of said printed circuit board have a different geometry with respect  
11          to one another as compared to a geometry of said first plurality of relatively parallel conductive paths in  
12          said first area.

1           9. The method of claim 8, wherein said rearranging is based on said analyzed at least  
2 one characteristic.

1           10. The method of claim 8, wherein said at least one characteristic comprises a timing  
2 relationship of signals along said first plurality of relatively parallel conductive paths.

1        11. The method of claim 10, wherein said timing relationship relates to one of push-out  
2 and pull-in of signal timings.

1        12. The method of claim 8, wherein said first plurality of relatively parallel conductive paths  
2 are on a first layer of said printed circuit board and said second plurality of relatively parallel conductive  
3 paths are on a second plane of said printed circuit board.

1        13. The method of claim 8, wherein said first plurality of relatively parallel conductive paths  
2 comprise a first plurality of traces on a first layer of said printed circuit board and said second plurality  
3 of relatively parallel conductive paths comprise a second plurality of traces on a second layer of said  
4 printed circuit board.

1        14. The method of claim 13, wherein said first plurality of traces are arranged on said first  
2 layer in a first ordered arrangement and said second plurality of traces are arranged on said second  
3 layer in a second ordered arrangement, and rearranging said pattern comprises determining said  
4 second ordered arrangement based on said analyzed at least one characteristic.

1        15. The method of claim 8, wherein said first plurality of relatively parallel conductive paths  
2 comprise a first plurality of vias coupling a first layer of said printed circuit board to a second layer of  
3 said printed circuit board, and said second plurality of conductive paths comprise a second plurality of  
4 vias coupling said first layer of said printed circuit board to said second layer of said printed circuit  
5 board.

1        16.      A method comprising:

2                analyzing a characteristic of a first plurality of conductive paths arranged in a first pattern; and  
3                altering said characteristic by rearranging said pattern.

1        17.      The method of claim 16, wherein said characteristic comprises a timing relationship of  
2        signals across said first plurality of conductive paths.

1        18.      The method of claim 17, wherein said timing relationship relates to one of push-out  
2        and pull-out of signal timings.

1        19.      The method of claim 16, wherein altering said characteristic comprises determining a  
2        second pattern for a second plurality of conductive paths based on said analyzed characteristic.

1        20.      The method of claim 19, wherein said first plurality of conductive paths are on a first  
2        plane and arranged in said first pattern and said second plurality of conductive paths are on a second  
3        plane and arranged in said second pattern.

1        21.      The method of claim 19, wherein said first plurality of conductive paths comprise a first  
2        plurality of traces on a first layer of a printed circuit board and said second plurality of conductive paths  
3        comprise a second plurality of traces on a second layer of said printed circuit board.

1        22. The method of claim 21, wherein said first plurality of traces are arranged on said first  
2 layer in a first ordered arrangement and said second plurality of traces are arranged on said second  
3 layer in a second ordered arrangement, and altering said characteristic comprises determining said  
4 second ordered arrangement based on said analyzed characteristics.

1        23. The method of claim 19, wherein said first plurality of conductive paths comprise a first  
2 plurality of vias coupling a first layer of a printed circuit board to a second layer of said printed circuit  
3 board, and said second plurality of conductive paths comprise a second plurality of vias coupling said  
4 first layer of said printed circuit board to said second layer of said printed circuit board.

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